Claims

[1] An array panel comprising:
an array portion formed on a first region of a substrate, the array portion accumulating and storing electrons generated in accordance with light supplied from outside; and
a gate-driving portion formed on a second region of the substrate, the gate driving portion applying a scanning signal for extracting the electrons to the array portion.

[2] The array panel of claim 1, wherein the gate-driving portion includes a plurality of stages sequentially making an electrical contact with each other, each of the stages including a plurality of thin film transistors comprising amorphous silicon, and including an input terminal and an output terminal through which corresponding signals are transmitted, a start signal being transmitted to the input terminal of a first stage, and an output signal of each stage being sequentially outputted from each output terminal, so that the stages function as a shift register.

[3] The array panel of claim 2, wherein each of the stages includes:
a pull-up portion that provides a corresponding signal to the output terminal among a first clock signal and a second clock signal, the second clock signal having a phase opposite to the phase of the first clock signal;
a pull-down portion that applies a first voltage to the output terminal;
a pull-up driver connected to an input node of the pull-up portion, the pull-up driver being turned on in accordance with the output signal of a previous stage, and being turned off in accordance with a first control signal so that the first clock signal or a second control signal is removedto remove the second clock signal; and
a pull-down driver connected to an input node of the pull-down portion, the pull-down driver being turned off in accordance with an input signal, and being turned on in accordance with the first control signal or the second control signal, wherein, the first clock signal and the first control signal are transmitted to odd numbered stages, and the second clock signal and the second control signal are transmitted to even numbered stages.

[4] An array panel comprising:
a substrate;

a gate line extended on the substrate in a first direction;
a data line extended on the substrate in a second direction;
a switching element including a gate electrode, a source electrode, and a drain electrode, the switching element being formed in a pixel region defined by the gate and the data lines;
a photoelectric cell for generating electrons in proportion with the intensity of light supplied from outside, thereby generating an electrical signal;
a pixel electrode formed in the pixel region, the pixel electrode gathering electrons generated from the photoelectric cell;
a storage capacitor formed in the pixel region, the storage capacitor storing the electrons gathered by the pixel electrode;
a gate driver making an electrical contact with an end portion of the gate line on the substrate, the gate driver sequentially providing a scan signal for driving the switching element; and
a data pad making an electrical contact with an end portion of the data line on the substrate, the electrons stored in the storage capacitor being extracted to the data pad through the switching element in case that the switching element is turned on.

[5] The array panel of claim 4, wherein the gate driver includes a plurality of stages sequentially making an electrical contact with each other, each stage including an input terminal and an output terminal through which corresponding signals are transmitted, a start signal being transmitted to the input terminal of a first stage, and an output signal of each stage being sequentially outputted from each output terminal, so that the stages function as a shift register.

[6] The array panel of claim 4, further comprising an organic layer interposed between the pixel electrode and the switching element.

[7] The array panel of claim 4, further comprising an organic layer interposed between the pixel electrode and the gate driver.

[8] The array panel of claim 4, wherein the pixel electrode comprises indium tin oxide (ITO).

[9] The array panel of claim 4, wherein the pixel electrode is disposed on a whole surface of the switching element.

[10] The array panel of claim 4, wherein the pixel electrode is disposed on a whole surface of the gate driver.

[11] A method of manufacturing an array panel, the method comprising:

forming first and second switching elements, a first conductive line for a data pad and a second conductive line for a storage capacitor, the first switching element corresponding to a pixel region of a substrate;

forming a first transparent electrode on the first and second conductive lines;

sequentially coating an insulating layer and an organic layer on the first transparent electrode;

partially removing the organic layer corresponding to the first and second conductive lines and a drain electrode of the first switching element;

partially removing the insulating layer corresponding to the first and second conductive lines, thereby exposing the data pad and drain electrode of the first switching element; and

forming a second transparent electrode for collecting electrons, the second transparent electrode being electrically connected to the data pad and the drain electrode.

[12] The method of claim 11,further comprising:

forming a protecting layer on the exposed organic layer and the second transparent layer;

forming a light conductive semiconductor layer on the protecting layer; and

forming an electrode on the light conductive semiconductor layer.

[13] The method of claim 11, wherein the second transparent electrode is disposed on a whole surface of the first switching element.

[14] The method of claim 11, wherein the second transparent electrode is disposed on a whole surface of the second switching element.

[15] The method of claim 11, wherein the second transparent electrode includes a plurality of stages sequentially making an electrical contact with each other, each of the stages including a plurality of thin film transistors comprising amorphous silicon, and including an input terminal and an output terminal through which corresponding signals are transmitted, a start signal being transmitted to the input terminal of a first stage, and an output signal of each stage being sequentially outputted from each output terminal, so that the stages function as a shift register.